METHOD OF MANUFACTURING FLASH MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of manufacturing semiconductor device, and more particularly, to a method of manufacturing flash memory device.

Background of the Related Art

In implementing the flash memory devices, shallow trench isolation (hereinafter called 'STI') is employed. In the prior art, as the sidewall oxidization process is employed, a tunnel oxide film formed at the top corner of the trench is formed in thickness thinner than a deposition target. The thickness of the tunnel oxide film formed at the top corner of the trench becomes thinner than that of the tunnel oxide film formed at its center. Furthermore, in order to sufficiently reduce the critical dimension (hereinafter called 'CD') in the active region, a photolithography technology of a micro line width is required. For this, expensive equipments are required and the cost price is thus increased. In addition, there are limitations in increasing the surface area of the floating gate and the capacitance value applied to the ONO (oxide/nitride/oxide) film being the dielectric film. Accordingly, it is difficult to expect an increase in the coupling ratio.

Furthermore, in manufacturing the flash memory device, a mask CD is changed and the uniformity of the wafer is poor, in a patterning process for isolating the floating gate. For this reason, it is not easy to implement a uniform floating gate. Accordingly, the coupling ratio is varied and fail occurs in a program or erase operation. Moreover, a mask work becomes more difficult in implementing a spacer of below 0.10 ㎛ in view of a higher-integrated design.

Meanwhile, if the floating gate is not uniformly formed, the difference in the coupling ratio is severe. Accordingly, an over-erase problem occurs in the program or erase operation of the cell, which adversely affects the characteristics of the device. Also, this causes to lower the yield and to increase the cost price due to an increased number of a mask process.

Incidentally, a device fail, etc. occurs due to a moat occurring in the STI or LOCOS process (indicating a shape that the field oxide film around the active region becomes depressed). In view of the above, it is an important problem that must be solved in a high-integrated flash memory device to secure a cell having no moat and increase the coupling ratio.

SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of manufacturing flash memory device capable of sufficiently reducing the critical dimension of the active region, increasing the surface area of the

floating gate, implementing a uniform and flat floating gate and prohibiting generation of a moat.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a method of manufacturing flash memory device according to the present invention is characterized in that it comprises the steps of (a) sequentially forming a tunnel oxide film, a first polysilicon film and a hard mask film on a semiconductor substrate, (b) etching the hard mask film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate through a patterning process to form a trench within the semiconductor substrate, (c) depositing an oxide film to bury the trench and then polishing the oxide film by means of a chemical mechanical polishing process until the hard mask film is exposed, (d) removing the hard mask film, (e) implementing a cleaning process so that a protrusion of the oxide film is recessed to an extent that the sidewall bottom of the first polysilicon film is not exposed, (f) depositing a second polysilicon film on the results in which the protrusion of the oxide film is recessed and then polishing the second polysilicon film until the protrusion

of the oxide film is exposed, (g) forming a dielectric film on the second polysilicon film, and (h) forming a control gate on the dielectric film.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

FIG. 1 ~ FIG. 11 are cross-sectional views of flash memory devices for explaining a method of manufacturing the memory device according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts. FIG. 1 ~ FIG. 11 are cross-sectional views of flash memory devices for explaining a method of manufacturing the memory device according to a preferred embodiment of the present invention.

Referring to FIG. 1, a semiconductor substrate 100 the top surface of

which is cleaned through a pre-treatment cleaning process is prepared. At this time, it is preferable that the pre-treatment cleaning process is implemented using DHF (diluted HF; solution where H_2O is mixed in a given ratio) and SC-1 (standard cleaning-1; solution where $NH_4OH/H_2O_2/H_2O$ solutions are mixed in a given ratio), or BOE (buffer oxide etchant; solution where $HF/NH_4F/H_2O$ solutions are mixed in a given ratio) and SC-1.

For the purpose of prohibiting crystal defects on the top surface of the semiconductor substrate 100 or surface process on it, a sacrificial oxide film 102 is formed on the semiconductor substrate 100. It is preferred that the sacrificial oxide film 102 is formed in a dry or wet oxidization mode and is formed in thickness of 70 Å ~ 100 Å at a temperature of about 750℃ ~ 800℃.

Ion implantation for forming wells and controlling the threshold voltage is implemented using the sacrificial oxide film 102 as a buffer layer. Ion implantation for forming the wells is implemented using a high energy. Ion implantation for controlling the threshold voltage is implemented using an energy lower than the energy used in ion implantation for forming the wells.

By reference to FIG. 2, the sacrificial oxide film 102 is removed. At this time, the sacrificial oxide film 102 may be removed using DHF and SC-1.

A tunnel oxide film 104 is formed on the results from which the sacrificial oxide film 102 is removed. It is preferable that the tunnel oxide film 104 is formed using a wet oxidization mode. For instance, the tunnel oxide film 104 may be formed by implementing wet oxidization at a temperature of about 750℃ ~ 800℃ and implementing annealing under nitrogen (N_2) atmosphere at a temperature of 900℃ ~ 910℃ for 20 ~ 30

minutes.

A first polysilicon film 106 to be used as a floating gate is deposited on the tunnel oxide film 104. The first polysilicon film 106 is formed by means of a low pressure-chemical vapor deposition (LP-CVD) method using a SiH_4 or Si_2H_6 gas. At this time, it is preferred that the first polysilicon film 106 is formed using an amorphous silicon film into which a dopant is not doped. Furthermore, it is preferred that the first polysilicon film 106 is formed in thickness of about 250 ~ 500 Å at a temperature of about 480 ~ 550 ℃ and a low pressure of about 0.1 ~ 3Torr.

A hard mask film 108 is formed on the first polysilicon film 106. The hard mask film 108 is formed using a silicon nitride film having an etch selectivity ratio to a trench oxide film (see '114' in FIG. 5). Furthermore, the hard mask film 108 is deposited by the LP-CVD method and is formed in thickness through which a protrusion of a trench oxide film 114 formed by a subsequent process is sufficiently protruded, for example, in thickness of about 1200 ~ 3500 Å.

Turning to FIG. 3, a trench 110 is formed into the semiconductor substrate 100 through patterning for forming an isolation film, thereby defining an isolation region and an active region. In the concrete, a photoresist pattern (not shown) defining the isolation region is formed. The hard mask film 108, the first polysilicon film 106, the tunnel oxide film 104 and the semiconductor substrate 100 are etched using the photoresist pattern as an etch mask, thus forming the trench 110. At this time, the trench 110 formed within the semiconductor substrate 100 is formed to have a slope (θ)

of a given angle. For instance, the trench 110 may be formed to have a slope of 75° ~ 88° .

A cleaning process is implemented in order to remove a native oxide film formed on the sidewall of the trench 110. The cleaning process may employ DHF and SC-1, or BOE and SC-1.

With reference to FIG. 4, in order to compensate for etch damage at the sidewall and bottom of the trench 110, make rounded the top and bottom corners of the trench 110 and reduce the CD in the active region, sidewall oxide films 112 are formed on the inner wall of the trench 110. At this time, it is preferred that the sidewall oxide films 112 are formed in a dry or wet oxidization mode and are formed in thickness of about 50~150Å at a temperature of 750~1150℃.

Referring to FIG. 5, a trench oxide films 114 is deposited to bury the trench 110. At this time, the trench oxide film 114 is deposited in thickness that is sufficiently deposited up to the top surface of the hard mask film 108 while burying the trench 110, for example, in thickness of about 5000~10000Å. It is preferred that the trench oxide film 114 is formed using a HDP (high density plasma) oxide film. The trench oxide film 114 is formed is buried so that void, etc. is not formed within the trench 110.

Thereafter, the trench oxide film 114 is polished by a chemical mechanical polishing process. It is preferred that the chemical mechanical polishing process is implemented until the hard mask film 108 is exposed.

After the chemical mechanical polishing process, a cleaning process is implemented to remove the trench oxide film 114 remaining on the hard mask

film 108. It is preferred that the cleaning process employs a BOE or HF solution and is controlled so that the trench oxide film 114 between the hard mask films 108 is not excessively recessed.

By reference to FIG. 6, the hard mask film 108 is removed. The hard mask film 108 may be removed using a strip process. For example, the hard mask film 108 may be removed using a phosphoric acid (H_3PO_4) solution.

With reference to FIG. 7, before a second polysilicon film (see '116' in FIG. 8) is deposited, the native oxide film formed on the first polysilicon film 106 is removed by means of a cleaning process using DHF and SC-1. The trench oxide film 114 is recessed by some degree and a desired space between the floating gates could be obtained, by means of the cleaning process. Further, it is preferred that the cleaning process is controlled so that the bottom of the sidewall of the first polysilicon film 106 is not exposed and a moat does not occur.

Referring to FIG. 8, a second polysilicon film 116 is deposited. The second polysilicon film 116 is formed by means of the LP-CVD (low pressure-chemical vapor deposition) method using a SiH_4 or Si_2H_6 gas and a PH_3 gas. It is preferred that the second polysilicon film 116 is formed using a polysilicon film into which a dopant is doped. At this time, the doped dopant may be phosphorous (P), etc. It is preferred that phosphorous (P) is doped at the dose of about 1.0E20～3.0E20 atoms/cc. Furthermore, it the second polysilicon film 116 is formed in thickness of about 1000 ~ 2000Å at a temperature of about 550 ~ 620℃ under a low pressure of about 0.1 ~ 3Torr.

By reference to FIG. 9, the second polysilicon film 116 is polished by

the chemical mechanical polishing until the trench oxide film 114 is exposed. By the polishing process, the second polysilicon film 116 is isolated by the trench oxide film 114.

Turning to FIG. 10, a cleaning process is implemented to etch the trench oxide film 114 protruded between the second polysilicon films 116 by a desired target. It is preferable that the cleaning process employs DHF or BOE. Thereby, the exposed area of the second polysilicon film 116 is increased while the sidewall of the second polysilicon film 116 contacting the protrusion of the trench oxide film 114, so that the coupling ratio could be increased.

With reference to FIG. 11, a dielectric film 124 is formed on the second polysilicon film 116 and the trench oxide film 114. It is preferred that the dielectric film 124 is formed to have a structure of an oxide film/nitride film/oxide film, i.e., the ONO ($SiO_2/Si_3N_4/SiO_2$) structure. The oxide (SiO_2) films 118 and 122 of the dielectric film 124 may be formed using high temperature oxide (HTO) using SiH_2Cl_2(dichlorosilane; DCS) and H_2O gas as a source gas. For instance, the oxide films 118 and 122 of the dielectric film 124 may be formed by means of the LP-CVD method under a low pressure of 0.1 ~ 3Torr at a temperature of about 810 ~ 850℃ using H_2O and SiH_2Cl_2(dichlorosilane; DCS) gas as a reaction gas. Furthermore, the nitride film 120 of the dielectric film 124 may be formed by means of the LP-CVD method under a low pressure of about 0.1 ~ 3Torr at a temperature of about 650 ~ 800℃ using NH_3 and SiH_2Cl_2(dichlorosilane; DCS) gas as a reaction gas. It is preferred that the first oxide film 118 is formed in thickness of

about 35 ~ 60 Å, the nitride film 120 is formed in thickness of about 50 ~ 65 Å and the second oxide film 122 is formed in thickness of about 35 ~ 60 Å.

Next, in order to improve the film quality of the ONO film and enhance the interface between the respective layers, a steam anneal process is implemented in a wet oxidization mode at a temperature of about 750 ~ 800 ℃. It is preferred that the process of forming the dielectric film 124 and the steam anneal process are implemented with no time delay between the respective processes in order to prevent contamination by the native oxide film or the impurities.

A third polysilicon film 126 to be used as a control gate is formed on the results on which the dielectric film 124 is formed. It is preferred that the third polysilicon film 126 is formed using an amorphous polysilicon film at a temperature of about 510 ~ 550 ℃ and a low pressure of about 0.1 ~ 3Torr. Furthermore, it is preferred that the third polysilicon film 126 is formed to have a dual structure on which a film into which a dopant is doped and a film into which a dopant is not doped are sequentially stacked, in order to prevent diffusion of fluorine (F) that may be substitutionally solidified into the dielectric film 124 to increase the thickness of the oxide film and prohibit formation of an abnormal film such as WP_x, etc. It is preferred that the thickness of the film into which the dopant is doped is about 1/3 ~ 6/7 of a total thickness (film into which the dopant is doped and film into which the dopant is not doped). The doped amorphous polysilicon film is formed by means of the LP-CVD method using a Si source gas such as SiH_4 or Si_2H_6 and a PH_3 gas. The undoped amorphous polysilicon film is formed by means of

an in-situ process immediately after supply of PH_3 gas is stopped. The third polysilicon film 126 is formed in thickness of about 500 ~ 1000 Å.

Thereafter, a silicide film 128 is formed on the third polysilicon film 126. At this time, it is preferred that the silicide film 128 is formed using a tungsten silicon (WSi) film. Furthermore, it is preferred that the tungsten silicon (WSi) film being the silicide film 128 is formed at a temperature between 300℃ ~ 500℃ using a reaction of SiH_4 (monosilane; MS) or SiH_2Cl_2(dichlorosilane; DCS) and WF_6 in order to obtain a low content of fluorine (F), a low stress after annealing, and a good adhesive strength. Also, it is preferred that the tungsten silicon (WSi) film is grown at the stoichiometry ratio of about 2.0 ~ 2.8 in order to implement an adequate step coverage and minimize the sheet resistance(Rs).

Next, an anti-reflective coating film (not shown) is formed on the silicide film 128. The anti-reflective coating film may be formed using SiO_xN_y or Si_3N_4.

Then, a gate patterning process is implemented. In other words, the anti-reflective coating film, the silicide film 128, the third polysilicon film 126 and the dielectric film 124 are patterned using a mask for forming a control gate. The second polysilicon film 116 and the first polysilicon film 106 are then patterned by means of a self-aligned etch process using the patterned anti-reflective coating film.

As described above, conventionally, there was a phenomenon that the thickness of the gate oxide film adjacent to the top corner of the trench is thinner than that of the center of the gate oxide film. On the contrary, the

present invention can prevent such phenomenon by applying the self-aligned STI technology. Furthermore, the present invention has advantageous effects that it can improve electrical characteristics such as retention fail, fast erase, etc. of the device since an active region so much as a desired CD could be obtained, and improve reliability of the device. Also, a uniform tunnel oxide film within a channel width could be kept by preventing the tunnel oxide film from being attacked. Therefore, the present invention can improve characteristics of the device.

Furthermore, the present invention has new effects that it can effectively secure the coupling ratio and easily secure a sufficient process margin, by freely adjusting the surface area of the floating gate.

In addition, the present invention has an advantageous effect that it can easily implement a flash memory device having a space of below 0.1 ㎛ in size, by use of a self-aligned floating gate process technology. Also, the present invention has new effects that it can minimize variation in the CD without resorting to the conventional method used in the mask process and the etch process, and implement a uniform floating gate over the entire wafer.

Also, the present invention has an advantageous effect that it can form a trench structure having no moat.

Incidentally, the present invention has a new effect that it is effective in improving retention characteristics since the interface with the ONO dielectric film is stable, by processing the second polysilicon film using a chemical mechanical polishing process.

Additionally, the present invention has an advantageous effect that it

can implement a flash memory device of a high reliability with a low cost, by using existing equipments and processes without using complex processes and additional equipments.

In the above description, it was described that one layer exists on the other layer. However, those having skill in the art will appreciate that one layer may exist immediately on the other layer and a third layer may be intervened between them.

The forgoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.